

Description

INTERLEVEL DIELECTRIC LAYER AND METAL LAYER SEALING

BACKGROUND OF INVENTION

[0001] Technical Field

[0002] The present invention relates generally to semiconductor fabrication, and more particularly, to methods for sealing an interlevel dielectric layer and metal layer.

[0003] Related Art

[0004] In semiconductor fabrication, processing requires two separate steps during generation of organic interlevel dielectric layers (ILDs) and metal layers in which the wafer is exposed to atmosphere including, for example, air, moisture, and possibly other chemicals. In particular, wafers are etched during via generation in such a way that organic ILD layers (e.g., SiLK by Dow Chemical) above the metal layer are opened and the metal layer is exposed to atmosphere when the wafer is moved between the etch

chamber and deposition chamber for the metallization of the vias. In these instances, the organic ILD layers adsorb contaminants from the atmosphere, which can be later released during processing of upper levels where the wafer is exposed to thermal treatment. When these contaminants are released, they diffuse toward the weak interface of metal and dielectric, and create a resistive layer that hinders the electrical connectivity. In addition, contaminants can diffuse to the exposed metal interface of, for example, copper (Cu), and create an oxide layer. The oxide layer affects the electrical contact with the upper level metal.

[0005] In view of the foregoing, there is a need in the art for way to eliminate exposure of organic ILD (such as SiLK) and metal layers to any undesired atmosphere.

SUMMARY OF INVENTION

[0006] The invention includes methods for eliminating exposure of organic ILD layers and metal layers after an etching step. The method includes etching through an ILD layer and leaving a portion of an underlying metal layer cap, maintaining the device in an inert gas, and depositing at least a portion of a liner into the opening to seal the ILD layer and the metal layer. Subsequent processing may in-

clude formation of a via by etching through the portion of the liner and the remaining portion of the cap layer, and depositing a metal.

[0007] A first aspect of the invention is directed to a method of preventing exposure of at least one layer of a semiconductor device, the method comprising the steps of: etching an opening through an interlevel dielectric (ILD) layer and leaving a remaining portion of an underlying cap layer; maintaining the semiconductor device in an inert gas; and forming a portion of a liner in the opening to prevent exposure of the ILD layer during subsequent processing.

[0008] A second aspect of the invention is directed to a method of forming a via in a semiconductor device, the method comprising the steps of: first etching an opening through an interlevel dielectric (ILD) layer and leaving a remaining portion of an underlying cap layer; maintaining the semiconductor device in an inert gas; forming at least a portion of a liner in the opening to prevent exposure of the ILD layer; second etching through the at least a portion of the liner and the portion of the underlying cap layer to expose a metal layer; and forming the via in the opening.

[0009] A third aspect of the invention is directed to a method of

forming a via in a semiconductor device, the method comprising the steps of: first etching an opening through an interlevel dielectric (ILD) layer and leaving a remaining portion of an underlying cap layer to maintain a metal layer thereunder sealed; maintaining the semiconductor device in an inert gas; degassing the semiconductor device; forming at least a portion of a liner in the opening to prevent exposure of the ILD layer in a chamber; second etching through the portion of the liner and the portion of the underlying cap layer to expose the metal layer in the chamber; and forming the via in the opening.

[0010] The foregoing and other features of the invention will be apparent from the following more particular description of embodiments of the invention.

BRIEF DESCRIPTION OF DRAWINGS

[0011] The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

[0012] FIG. 1 shows a first step of the method according to the invention.

[0013] FIG. 2 shows a second step of the method according to the invention.

[0014] FIG. 3 shows a third step of the method according to the

invention.

[0015] FIG. 4 shows a fourth step of the method according to the invention.

DETAILED DESCRIPTION

[0016] With reference to the accompanying drawings, FIGS. 1–4 show schematic cross-sectional representations of methods of preventing exposure of at least one layer of a semiconductor device and generating a via according to the invention.

[0017] In FIG. 1, a substrate 10 is illustrated including a representative first interlevel dielectric (ILD) layer 12 thereon. Subsequent layers include a metal layer (M1) 14 on organic ILD layer 12, a metal layer cap layer 16 over metal layer 14 and another second organic ILD layer 18. Each layer may include any now known or later developed material used for the layer's respective purpose. In one embodiment, for example, substrate 10 may include silicon, ILD layers 12, 18 may include an organic low-k material such as SiLK by Dow Chemical, cap layer 16 may include silicon nitride (SiN) or silicon carbide (SiC), and metal layer 14 may include copper (Cu). It should be recognized that the material makeup of the layers may vary and not depart from the scope of the invention.

[0018] FIGS. 1–2 illustrate a method of preventing exposure of at least one layer of a semiconductor device; and FIGS. 1–4 illustrate a method of forming a via in a semiconductor device.

[0019] In a first step of the method, shown in FIG. 1, an opening 40 is etched through an organic interlevel dielectric (ILD) layer 18, leaving a remaining portion 42 of an underlying cap layer 16. In one embodiment, remaining portion 42 is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness. Subsequent to this step, the semiconductor device is maintain in an inert gas, e.g., argon (Ar), nitrogen (N), helium (He), xenon (Xe). If necessary, a degassing step for the device may be conducted at this point.

[0020] Referring to FIG. 2, a next step includes forming a portion 44 of a liner 46 in the opening 40 to prevent exposure of ILD layer 18 during subsequent processing. In one embodiment, portion 44 of liner 46 is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness, and preferably no less than approximately 10% of the total liner thickness and no greater than approximately 20% of the

total liner thickness. Liner 46 includes any now known or later developed liner material including, for example, tantalum nitride, tantalum, or other refractory metals.

[0021] Subsequent processing to the sealing steps may include formation of a via as follows:

[0022] In FIG. 3, portion 44 of liner 46 and portion 42 of cap layer 16 are etched to expose metal layer 14. This etching step may be conducted in an etching chamber to which the semiconductor device is moved, or it may be conducted in the same liner deposition chamber in which the liner formation step occurs.

[0023] In FIG. 4, a via 50 is formed in the opening, for example, by depositing a metal such as copper (Cu). Subsequent processing to planarize the surface (not shown) may also be required.

[0024] The above-described invention seals organic ILD layer 18 from the atmosphere and also metal layer 14 during and after degas (if provided). In addition, portion 44 of liner 46 is a "bottomless liner" which prevents, if required by the integration scheme, an excessive argon (Ar+) cleaning step.

[0025] While this invention has been described in conjunction with the specific embodiments outlined above, it is evi-

dent that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims.

[0026] What is claimed is: